Amendments to the Specification:

Please replace page 11 lines 12-20 with the following amended lines:

Figure 2B illustrates a side view of a deep N-well region coupled to N-Well_1 and N-well_2 in accordance with an embodiment of the present invention, showing the routing of the body-bias voltage. As illustrated in Figure 2B, there is a first sub-surface conductive boundary ~~396~~ 397 between N-Well_1 and deep N-well region 310. Moreover, there is a second sub-surface conductive boundary ~~397~~ 396 between N-well_2 and deep N-well region 310. Surface N-well_1 has a PFET 370. Also, surface N-well_2 has a PFET 370. The P-well region has an NFET 380 and separates N-well_1 and N-well_2. The body-bias voltage Vnw is routed to N-well_1 and N-well_2 via the first and second sub-surface conductive boundaries 396 and 397.

Please replace page 24 line 15 to page 25 line 2 with the following amended lines:

Figure 8A illustrates a top view of multiple axial deep N-well (ADNW) regions forming a first axial sub-surface strip structure 800A in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 810A-810D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Axial deep N-well regions 810A-810D are formed in a first parallel orientation. The first parallel orientation is ~~parallel~~ substantially perpendicular to surface N-well

regions (e.g., N-well_G, N-well_H, and N-well_I). In this case, the combination of surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I) and first axial sub-surface strip structure 800A forms a mesh-type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.

Please replace page 26 lines 1-11 with the following amended lines:

Figure 8B illustrates a top view of multiple axial deep N-well (ADNW) regions forming a second axial sub-surface strip structure 800B in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 812A-812D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Axial deep N-well regions 812A-812D are formed in a second parallel orientation. The second parallel orientation is ~~parallel~~ substantially perpendicular to surface N-well regions (e.g., N-well_J, N-well_K, and N_well_L). In this case, the combination of surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L) and second axial sub-surface strip structure 800B forms a mesh-type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.